IN THE CLAIMS

1. (Currently amended) A method for writing data ~~(DATA)~~ from a processor ~~(603)~~ to a non-volatile memory ~~(602)~~ embedded in an integrated circuit, comprising the following steps (a) at least part of said data ~~(DATA)~~ to be written to said non-volatile memory ~~(602)~~ is transferred to a volatile memory ~~(601)~~, (b) when said data ~~(DATA)~~ has been transferred to said volatile memory ~~(601)~~, a wait signal ~~(wait)~~ is sent to said processor ~~(603)~~, (c) said part of said data ~~(DATA)~~ is transferred from said volatile memory ~~(601)~~ to said non-volatile memory ~~(602)~~, (d) said wait signal (wait) is removed.

2. (Currently amended) The method for writing data according to claim 1, wherein the data transfer to said volatile memory and to said non-volatile memory is controlled by an interface ~~(605)~~.

3. (Currently amended) The method for writing data according to claim 1 ~~or 2~~, wherein at the beginning of the data transfer from the volatile memory ~~(601)~~ to the non-volatile memory ~~(602)~~, said non-volatile memory ~~(602)~~ is set in write mode.

4. (Currently amended) The method for writing data according to ~~any of the preceding claims~~claim 1, wherein during the data transfer from the volatile memory ~~(601)~~ to the non-volatile memory ~~(602)~~, said non-volatile memory ~~(602)~~ is set in program mode.

5. (Currently amended) The method for writing data according to ~~any preceding claim~~claim 1, wherein at the end of the data transfer from the volatile memory ~~(601)~~ to

the non-volatile memory ~~(602)~~, said non-volatile memory ~~(602)~~ is set in read mode.

6. (Currently amended) The method for writing data according to ~~any preceding claim~~claim 1, wherein all of the data ~~(DATA)~~ is transferred first to the volatile memory ~~(601)~~.

7. (Currently amended) The method for writing data according to ~~any preceding claim~~claim 1, wherein the addresses ~~(ADDR)~~ corresponding to the data ~~(DATA)~~ to be written to the non-volatile memory ~~(602)~~ are stored intermediately.

8. (Currently amended) The method for writing data according to ~~any preceding claim~~claim 1, wherein before the data ~~(DATA)~~ is written to the volatile memory ~~(601)~~, the wait signal ~~(wait)~~ is sent to the processor ~~(603)~~ and is removed after said data ~~(DATA)~~ is completely written to said volatile memory ~~(601)~~.

9. (Currently amended) An integrated circuit with a processor ~~(603)~~, a volatile memory ~~(601)~~, a non-volatile memory ~~(602)~~, and an interface ~~(605)~~ connecting said processor ~~(603)~~ to said volatile memory ~~(601)~~, and said non-volatile memory ~~(602)~~ to said volatile memory ~~(601)~~, wherein said interface ~~(605)~~ is equipped: to transfer data ~~(DATA)~~ to be written to said non-volatile memory ~~(602)~~ first to said volatile memory ~~(601)~~, to send a wait signal ~~(wait)~~ to said processor ~~(603)~~ when said data ~~(DATA)~~ is transferred to said volatile memory ~~(601)~~, to transfer said data ~~(DATA)~~ from said volatile memory ~~(601)~~ to said non-volatile memory ~~(602)~~, and to remove said wait signal ~~(wait)~~.

10. (Currently amended) The integrated circuit according to claim 9, wherein the non-volatile memory ~~(602)~~ is a flash memory.

11. (Currently amended) The integrated circuit according to claim 9 ~~or 10~~, wherein the volatile memory ~~(601)~~ is a random access memory or a static random access memory.

12. (Currently amended) The integrated circuit according to claim 9~~, 10 or 11~~, wherein the volatile memory ~~(601)~~ is an embedded volatile memory.